An Advanced Approach to Power Module Packaging

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Abstract

The advanced power electronic packaging technology developed at GE CRD eliminates the need for wire bonds, offers low inductance strip-lined power electrodes, and low parasitic impedance. In addition, the planarity of the top layer structure and the thermal base provide double-sided cooling capability and improve the size, weight, cost, and thermal and electrical performance of the package.

Introduction

The advanced Chip on Flex Power Overlay Technology (POL) offers significant advantages over the state of the art power modules available on the market to day. Higher packaging density, lower package parasitics, higher reliability, lower weight and size and higher efficiency are among the key advantages of this technology.

One of the most important features of the POL is the elimination of bond wires. The power and control circuit to device interconnections is achieved through metalized through holes. This approach dramatically reduces the interconnect length, interconnect parasitics, and increases packaging density by allowing us to pack power devices more closely.

Another extremely important feature of the POL is the double-sided integral heat exchanger design. Thermally, the chip on flex approach creates a planar interface that makes it possible to remove the heat from the topside of the module. The low thermal resistance of the top side path between the heat sink and the top layer of the power devices where most of the heat generation takes place offers improved thermal performance compare to cooling through the back side of power devices. It is also now possible to employ double sided cooling which can more than double the thermal performance of power module. Therefore, the improved thermal performance strongly couples with and complements the no wire bond approach allowing us to take full advantage of the POL

Because of these, two key features and fully striplined power electrode design the module EMI will be significantly lowered and the module efficiency will be improved. A natural outcome of these enhancements is the ability to switch the advanced power devices at higher speeds and frequencies without pushing the limits of SOA of power devices. The reduced parasitics, particularly reduced L di/dt noise will allow us to use power devices with lower breakdown voltage, which improves both the cost and the electrical efficiency of modules. Ultimately the size weigh and the cost of passive filter components will also go down.

A Cost effective fabrication approach

The CF POL technology is designed to make use of the commercially available materials, processes and equipment wherever possible. The manufacturability, cost and reliability factors were incorporated early in the design. The following paragraphs describe the various steps of the fabrication technology.

Step 1. A thin layer of organic dielectric sheet is attached to a carrier frame, figure 1. The carrier frame will offer a convenient way for transport, ease of handling and dimensional stability. The thermal, structural and electrical properties of the specific dielectric film are compatible with the cost, reliability and the performance goals. The low modulus (high compliance), low CTE of the dry film dielectric improve the thermal/structural reliability of the power module.

Figure1. The dry film dielectric is attached to a ring shaped carrier frame

Step 2. The via pattern for device power and control connections are made by a laser or mechanical punch. Figure 2. The stretched dielectric membrane contains multiple power modules. The frame improves the dimensional stability of the membrane allowing a tighter

spacing for vias. Increased via density reduces the resistive losses and current crowding.

Figure 2) Form 0.020" diameter vias on 0.050" staggered centers (a typical configuration)

Step 3. A partially cured polymer resin (bond layer) is applied to dry film dielectric sheet (a membrane). The bond layer is typically a ~ 0.0005 inch thick layer of acrylic or epoxy resin, Figure 3. The bond layer and a protective release layer may be attached to the membrane before the formation of the via holes for the power interconnect. Alternately, the bond layer may be applied after forming the vias.

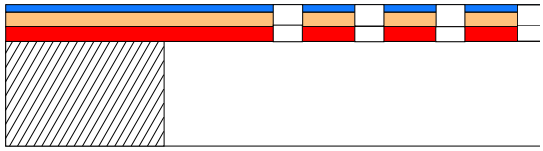

Figure 3) A partially cured B-stage bond layer is applied over the membrane

Step 4. Pick and place the power devices down on the glue layer. Cure the glue layer in a vacuum oven under low pressure to achieve bonding of power devices to the membrane. Note that during the cure process some resin from the bond layer will be squeezed in to the hole covering the device metalization as a ring of cured resin. The effect of this ring of cured resin will depend on the ratio of the width of the ring to the diameter of the hole. The exposed cure resin needs to be cleaned before further processing, if this ratio is 0.2 or higher.

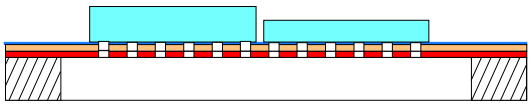

Figure 4. Pick and place power devices over the glue layer. To achieve bonding, cure the bond layer in a vacuum oven

Step 5. Sputter clean the residual glue layer and the thin aluminum oxide layer from the standard top layer metalization (Al) of all power devices. Blanket sputtering of a layer of adhesion metal and a layer of conductive metal over the Al metalization follows the cleaning process. The adhesion and conductive metal layers are usually Ti and Cu, respectively, figure 5. Subsequently, an approximately 0.005 inch thick conductive Cu layer is electroplated over the sputtered Cu seed layer. The plated blanket Cu layer then subtractively patterned to form the power and the control circuit and their I/O pads.

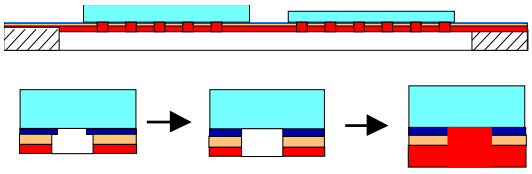

Figure 5. RIE or sputter clean the excess polymer layer and the aluminum oxide layer, blanket metalize with Ti and Cu, plate up with Cu and pattern

Step 6. In step 6 the power devices will be connected to an electrically insulating but thermally conducting base plate. This base will be fabricated by metalizing an approximately 0.040 inch thick AlN plate by Cu and CuMo30 infiltrated composite from both the front and the back side as shown in the Figure 6. The standard solderable backside metalization of the power devices will be bonded to Cu metalization of the power circuit formed over the AlN thermal base.

The second layer of the power circuit will be fabricated by directly active brazing one or multiple, physically separated layers of Cu sheets with different thickness to the AlN thermal plate. The over sized Cu sheets will be etched to provide a design specific pattern consisting of three or more different thickness, and the power and control electrodes. The thickness will include the full and a fraction of the original Cu sheet(s), and zero Cu thickness. The selective etch process will be carried out in multiple steps that will provide the circuit pattern and the desired thickness variations. The thickness variations will accommodate the variation in the thickness of different types of power devices fabricated by different suppliers. The approach can easily accommodate the thickness variations up to 0.015 inch in a stepwise fashion. The screened and reflowed solder thickness (≈ 0.003 inch) will help to

accommodate the statistical variations in the thickness of power devices and the thickness of the etched layers both of which is usually less than +/- 0.001 inch.

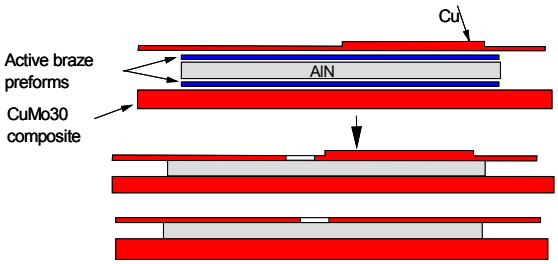

Figure 6. Insulating thermal base fabrication: active brazed partially and fully etched Cu and infiltrated CuMo composite sheets on AlN base plates

It is important to note that the selective etch process is required only if double sided cooling approach is necessary or the current density is more than what ~.005 inch thick plated up Cu can support (~1000Amp). Otherwise, the flexible POL can accommodate differences in device height.

Advantageously, due to the planarity, this structure provides a double-sided cooled module design. Double-sided cooling takes advantage of the planarity of the top (first) layer of the power circuit. The top layer power circuit can be mirror-imaged on an oversized copper sheet of the upper thermal base assembly that is actively brazed to an Aluminum Nitrate plate, as described above. Since such a copper metalization can carry the required current levels, the thickness of the plated-up Cu layer may be significantly reduced.

The metalized and patterned membrane carrying the power devices are then situated between the copper-metalized aluminum nitride sheets and soldered in a single or two step, fluxless soldering process in a reducing atmosphere

For a non-hermetic commercial power module design, the copper-metalized aluminum nitride thermal plates are attached to infiltrated CuMo30 composite plates. An exemplary thickness of copper-molybdenum plates is in the 0.050 inch to 0.100-inch range, as determined by the module size and stiffness requirements.

Summary

A new approach to packaging high performance power devices was presented. It was shown that the GE's cost effective POL Power packaging technology is ideally suited for high heat flux and high performance applications. This is primarily due to the elimination of bond wires and the planar geometry which offers cooling of power devices from top, bottom or both sides of the power module. It was also shown that a cost effective, scaleable high performance integral heat exchanger can maximizes the thermal performance of POL technology thereby helping to utilize its full potential.

Due to the excellent thermal and electrical performance, low weight, volume, and cost effectiveness GE's revolutionary POL technology sets a new standard for the future of Packaging Power Electronics Modules.

Acknowledgements

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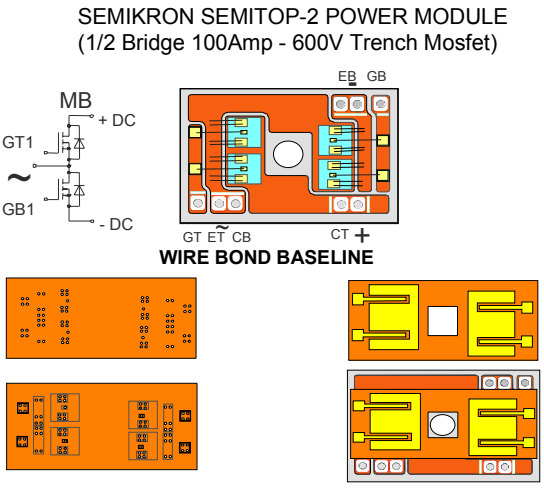
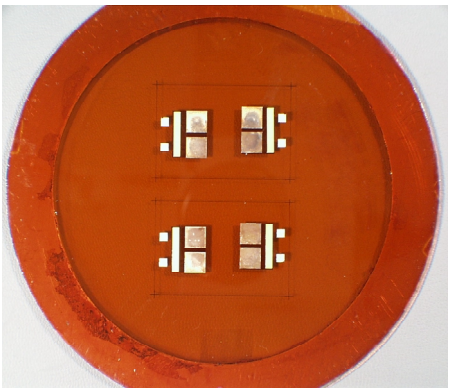
Last but not the least; the authors would like to thank Paul McConnelee and Mustansir Kheraluwala for their valuable support during the development of POL.

APPENDIX:
A POL version of a commercial module:

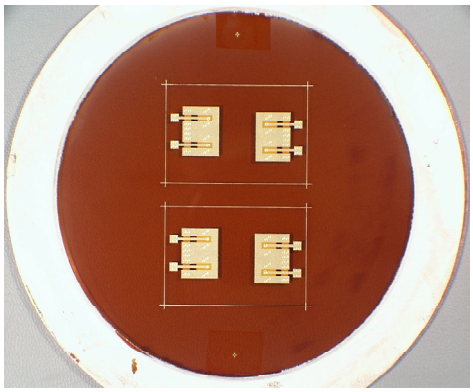
As a part of commercialization efforts, the POL technology was transferred to V. Tech packaging laboratory directed by Prof. Guo-Quan Lu. The POL approach is among the leading candidates of standard technology for future power modules by CPES consortium.
As a demonstration vehicle, GE CRD built a fully functional POL version of the Semikron's commercial Semitop-2 power module (half bridge 200 A, 600 V Mosfet version), see Figures 1A. More recently a 200A, 1200V IGBT version of the same module was built by V-Tech packaging laboratory.



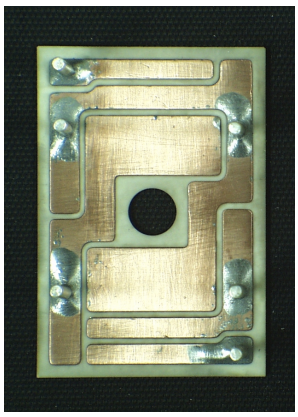
Finished COF POL Frames for Semikron's Semitop-2 Power Module



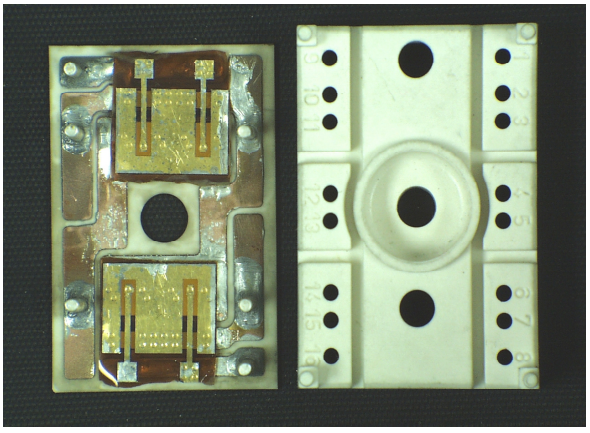
Device side



Power Circuit side



Pin Attached



POL soldered on the base

Figure 1A. A POL version of the Semitop-